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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF FOR THE APPELLANT

Ex parte TIRKKONEN

POWER ALLOCATION IN A COMMUNICATION SYSTEM

Serial No. 10/632,089
Appeal No.:
Group Art Unit: 2618

Enclosed is a check in the amount of Five Hundred Dollars ($500.00) to cover the official fee for this Appeal Brief. In the event that there may be any fees due with respect to the filing of this paper, please charge Deposit Account No. 50-2222.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Appellant:

Olav TIRKKONEN et al. Appeal No.:

Serial Number: 10/632,089 Group Art Unit: 2618

Filed: August 1, 2003 Examiner: Duc M. Nguyen

For: POWER ALLOCATION IN A COMMUNICATION SYSTEM

BRIEF ON APPEAL

February 23, 2007

I. INTRODUCTION

This is an appeal from the final rejection set forth in an Official Action dated June 20, 2006, finally rejecting claims 1-23, all of the claims pending in this application, as being unpatentable over Sadjadpour et al. (U.S. Publication No. 2001/0055332) in view of Applicants' admitted prior art (AAPA) and Kim et al. (U.S. Publication No. 2003/0128769). A Request for Reconsideration was timely filed on November 20, 2006. An Advisory Action was issued on December 8, 2006, indicating that for purposes of appeal, the proposed amendments would be entered. A Notice of Appeal was timely filed on December 20, 2006 with petition for Extension of Time. This Appeal Brief is being timely filed.

II. REAL PARTY IN INTEREST

The real parties in interest in this application are Nokia Corporation, of Espoo, Finland, by virtue of an Assignment which was submitted for recordation on December

18, 2003, and which was recorded at Reel 014810, Frame 0650, on December 19, 2003.

III. STATEMENT OF RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences which will directly effect or be directly effected by or have a bearing on the Board's decision in this appeal.

IV. STATUS OF CLAIMS

Claims 1-23, all of the claims pending in the present application are the subject of this appeal. Claims 1, 18, and 23 were rejected under 35 USC 102(a) as being anticipated by *Sadjadpour* (U.S. Patent Publication No. 2001/0055332). Claims 2-13, 19, 20, and 22 were rejected under 35 USC 102(a) as being unpatentable over *Sadjadpour*, in view of Applicants' admitted prior art (AAPA). Claims 14-17, and 21 were rejected under 35 USC 103(a) as being obvious over *Sadjadpour*, in view of AAPA, and further in view of *Kim* (U.S. Patent Publication No. 2003/0128769).

V. STATUS OF AMENDMENTS

Claim 1 was amended in a response filed on November 20, 2006. The Advisory Action dated December 8, 2006 indicated that the amendment would be entered for purposes of Appeal. No further amendments have been made. Claims 1-23 are currently pending.

VI. SUMMARY OF CLAIMED SUBJECT MATTER

The independent claims involved in this appeal are claims 1, 18-20, 22, and 23.

Claim 1, upon which claims 2-17 are dependent, recites a communication system for transferring data between a transmitter and a receiver over a plurality of channels (Specification, paragraph 0022, Figures 1-3). The communication system includes modulation circuitry having a plurality of modulation alphabets providing a set of a bit loading sequences (Specification, paragraphs 0022, 0036, Figures 1-3). The system further includes circuitry configured to determine a power allocation for at least one bit loading sequence based on minimizing an error rate (Specification, paragraphs 0022, 0037, 0043, 0050-0054, Figures 1-3), and circuitry configured to select a bit loading sequence with a lowest error rate (Specification, paragraphs 0022, 0055-0056, Figures 1-3).

Claim 18 recites a method for transferring data between a transmitter and receiver over a communication channel (Specification, paragraph 0025). The method includes identifying a set of bit loading sequences from a plurality of modulation alphabets (Specification, paragraphs 0025, 0036, Figures 1-3), determining a power allocation for at least one bit loading sequence based on minimizing an error rate (Specification, paragraphs 0025, 0037, 0043, 0050-0054, Figures 1-3), and selecting a bit loading sequence with a lowest error rate and applying the power allocation to at least one communication channel (Specification, paragraphs 0025, 0055-0056, Figures 1-3).

Claim 19 recites a communication system for transferring data between a transmitter and receiver over a communication channel (Specification, paragraphs 0026, Figures 1-3). The system includes a first circuitry means for decomposing a communication channel into a plurality of logical channels (Specification, paragraphs 0026, 0032, Figures 1-3), and a modulation circuitry having a plurality of modulation

alphabets, at least two modulation alphabets are capable of representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels (Specification, paragraphs 0026, 0036-0037, Figures 1-3). The circuitry also includes a second circuitry means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences (Specification, paragraphs 0026, 0043, 0050-0054, Figures 1-3), and a third circuitry for choosing a bit loading sequence having a minimum bit error rate (Specification, paragraphs 0026, 0055-0056, Figures 1-3).

Claim 20, upon which claim 21 is dependent, recites a method for transferring data between a transmitter and receiver over a communication channel (Specification, paragraph 0027, Figures 1-3). The method includes decomposing a communication channel into a plurality of logical channels (Specification, paragraphs 0027, 0032, Figures 1-3), and selecting from a plurality of modulation alphabets, wherein at least two modulation alphabets for modulating data are capable of representing the data using a different number of bits (Specification, paragraphs 0027, 0036, Figures 1-3). The method further includes identifying a set of bit loading sequences for a fixed data rate which specify a number of bits to be loaded onto corresponding logical channels of the plurality of channels (Specification, paragraphs 0027, 0037, Figures 1-3), allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences (Specification, paragraphs 0027, 0043, 0050-0054, Figures 1-3), and choosing a bit loading sequence

having a minimum bit error rate (Specification, paragraphs 0027, 0055-0056, Figures 1-3).

Claim 22 recites a communication system for transferring data between a transmitter and receiver over a communication channel (Specification, paragraph 0027, Figures 1-3). The system includes a decomposing means for decomposing a communication channel into a plurality of logical channels (Specification, paragraphs 0027, 0032, Figures 1-3), and a representing means for representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels (Specification, paragraphs 0027, 0036-0037, Figures 1-3). The system further includes an allocating means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences (Specification, paragraphs 0027, 0043, 0050-0054, Figures 1-3), and a choosing means for choosing a bit loading sequence having a minimum bit error rate (Specification, paragraphs 0027, 0055-0056, Figures 1-3).

Claim 23 recites a communication system for transferring data between a transmitter and a receiver over a plurality of channels (Specification, paragraph 0022, Figures 1-3). The communication system includes a providing means for providing a modulation circuitry having a plurality of modulation alphabets and for providing a set of a bit loading sequences (Specification, paragraphs 0022, 0036, Figures 1-3). The system further includes a determining means for determining a power allocation for at least one bit loading sequence based on minimizing an error rate (Specification, paragraphs 0022, 0037, 0050-0054, Figures 1-3), and selecting means for selecting a bit

loading sequence with a lowest error rate (Specification, paragraphs 0022, 0055-0056, Figures 1-3).

VII. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are the rejection of claims 1, 18, and 23 under 35 USC 102(a) as being anticipated by *Sadjadpour* (U.S. Patent Publication No. 2001/0055332), claims 2-13, 19, 20, and 22 under 35 USC 102(a) as being unpatentable over *Sadjadpour*, in view of Applicants' admitted prior art (AAPA), and claims 14-17, and 21 under 35 USC 103(a) as being obvious over *Sadjadpour*, in view of AAPA, and further in view of *Kim* (U.S. Patent Publication No. 2003/0128769).

VIII. APPELLANT'S ARGUMENTS

Appellants respectfully submit that each of pending claims 1-23 recites subject matter that is not taught, disclosed, or suggested by the cited art. Each of the claims is being argued separately, and thus, each of the claims stands or falls alone.

A. Claims 1, 18, and 23 are novel in view of *Sadjadpour*

In the final Office Action, claims 1, 18, and 23 were rejected under 35 U.S.C. §102(a) as being anticipated by *Sadjadpour* (U.S. Publication No. 2001/0055332). The Office Action took the position that *Sadjadpour* teaches each and every element recited in the claims. Appellants submit that each of claims 1, 18, and 23 recite subject matter that is not taught or disclosed by *Sadjadpour*, and as such, the Board's reversal of the rejection is respectfully requested.

1) Claim 1

Claim 1 recites a communication system for transferring data between a transmitter and a receiver over a plurality of channels. The communication system includes modulation circuitry having a plurality of modulation alphabets providing a set of a bit loading sequences. The system further includes circuitry configured to determine a power allocation for at least one bit loading sequence based on minimizing an error rate, and circuitry configured to select a bit loading sequence with a lowest error rate.

Appellants respectfully submit that claim 1 recites subject matter which is neither disclosed nor suggested by *Sadjadpour*.

Sadjadpour discloses a discrete multi-tone modem that operates to minimize cross talk over a twisted pair cable. The spectrum of the twisted pair cable can be split into multiple sub-bands or QAM channels, where each channel is able to handle K*i* bits of data, where *i* is the member of the channel (*Sadjadpour*, paragraph [0027]). The bit addition algorithm of *Sadjadpour* describes how an array of different bit allocation settings are ordered in ascending order so that bit allocation can be determined based on the least possible power for the maximum data rate possible or a desired data rate (*Sadjadpour*, paragraphs [0037]-[0038]). Bits are then added and the process continued until the addition of any further bit in any of the frequency bins violates at least one predetermined constraint, such as power budget, power mask, or maximum number of bits per frame, for example. Further, in another described embodiment of *Sadjadpour*, the method of allocating bits is modified by modifying the incremental power term by a weighting dependent on the frequency of the tone (sub-frequency).

Appellants note that a "claim is anticipated only if each and every element as set

forth in the claim is found, either expressly or inherently described, in a single prior art reference" *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Additionally, the "identical invention must be shown in as complete detail as is contained in the...claim" *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Appellants respectfully assert that the final Office Action has failed to meet these requirements.

In other words, Appellants submit that the final Office Action has failed to establish a prima facie case for anticipation as *Sadjadpour* fails to disclose each and every element of claim 1. For example, *Sadjadpour* does not teach or suggest "circuitry configured to determine a power allocation for at least one bit loading sequence based on minimizing an error rate" and "circuitry configured to select a bit loading sequence with a lowest error rate," as recited in claim 1.

The Office Action took the position that *Sadjadpour* disclosed, at paragraphs 0043-0046, modulation circuitry having a plurality of modulation alphabets providing a set of bit loading sequences, circuitry configured to determine power allocation for at least one bit loading sequence based on minimizing an error rate, and circuitry configured to select a bit loading sequence with a lowest error rate, as recited in Appellants' claim 1. However, Appellants respectfully submit that no such disclosure exists in *Sadjadpour*. Paragraphs 0043-0046 of *Sadjadpour* are directed to Figure 6 thereof, and they are directed to blocks 61-68 representing various objective functions that can be identified from various algorithms. Function 64 is directed to representing minimization of an arbitrary function of total power and maximization of total data rate. Block 61 of *Sadjadpour* illustrates functions which can apply joined minimization of the cross talk and

maximization of the total data rate. A further discussion of this aspect of *Sadjadpour* can be found in paragraphs 39-42 thereof.

Therefore, *Sadjadpour* only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. *Sadjadpour*, however, fails to disclose or suggest circuitry configured to select a bit loading sequence with the lowest error rate. Appellants respectfully submit that there is simply no disclosure or suggestion in *Sadjadpour* of any elements which could be comparable to the circuitry as recited in claim 1, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate. As discussed above, and as discussed in Appellants' previous responses, the present invention is directed to a device which contains circuitry and which can perform a step of selecting a bit loading sequence based on a lowest error rate.

Furthermore, Appellants submit that *Sadjadpour* fails to teach or suggest "circuitry configured to determine a power allocation for at least one bit loading sequence based on minimizing an error rate," as recited in claim 1. As noted above, *Sadjadpour* does not teach or disclose power allocation for bit loading frequencies based on minimizing the error rate; rather, *Sadjadpour* discloses only power allocation based only on reducing the cross talk. There is no teaching or suggestion in *Sadjadpour* of power allocation for bit loading frequencies based on minimizing the error rate, and as such, Appellants submit that it is incorrect for the final Office Action to suggest or conclude, without specific citation to the prior art, that *Sadjadpour* teaches power allocation for bit

loading frequencies based on minimizing the error rate when only cross talk is discussed in *Sadjadpour*.

For at least the reasons discussed above, Appellants submit that *Sadjadpour* fails to disclose or suggest all of the elements of claim 1. Accordingly, the Board's consideration and reversal of the rejection thereof is respectfully requested.

2) Claim 18

Claim 18 recites a method for transferring data between a transmitter and receiver over a communication channel. The method includes identifying a set of bit loading sequences from a plurality of modulation alphabets, determining a power allocation for at least one bit loading sequence based on minimizing an error rate, and selecting a bit loading sequence with a lowest error rate and applying the power allocation to at least one communication channel.

Appellants respectfully submit that claim 18 recites subject matter which is neither disclosed nor suggested by *Sadjadpour*.

As discussed above, *Sadjadpour* discloses a discrete multi-tone modem that operates to minimize cross talk over a twisted pair cable. The spectrum of the twisted pair cable can be split into multiple sub-bands or QAM channels, where each channel is able to handle K*i* bits of data, where *i* is the member of the channel (*Sadjadpour*, paragraph [0027]). The bit addition algorithm of *Sadjadpour* describes how an array of different bit allocation settings are ordered in ascending order so that bit allocation can be determined based on the least possible power for the maximum data rate possible or a desired data rate (*Sadjadpour*, paragraphs [0037]-[0038]). Bits are then added and the process continued until the addition of any further bit in any of the frequency bins violates

at least one predetermined constraint, such as power budget, power mask, or maximum number of bits per frame, for example. Further, in another described embodiment of *Sadjadpour*, the method of allocating bits is modified by modifying the incremental power term by a weighting dependent on the frequency of the tone (sub-frequency).

Appellants note that a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Additionally, the "identical invention must be shown in as complete detail as is contained in the...claim" *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Appellants respectfully assert that the final Office Action has failed to meet these requirements.

In other words, Appellants submit that the final Office Action has failed to establish a prima facie case for anticipation as *Sadjadpour* fails to disclose each and every element of claim 18. For example, *Sadjadpour* does not teach or suggest "determining a power allocation for at least one bit loading sequence based on minimizing an error rate" and "selecting a bit loading sequence with a lowest error rate and applying the power allocation to at least one communication channel," as recited in claim 18.

The Office Action took the position that *Sadjadpour* disclosed, at paragraphs 0043-0046, the above-recited limitations of claim 18. However, Appellants respectfully assert that no such disclosure exists in *Sadjadpour*. These paragraphs of *Sadjadpour*, which describe Figure 6, show the various inputs which are required in order to operate the bit allocation algorithm. Thus, blocks 61-68 represent the various objective functions with the shaded blocks of Figure 6 being those used to reduce the cross talk. Function

64 represents the joint minimization of an arbitrary function of the total power and maximization of the total data rate such as would be achieved using the algorithm described in paragraphs 0036-0038. Similarly, function block 61 shows the functions which apply joint minimization of the cross talk and maximization of the total data rate, as is shown in the method described in paragraphs 0039-0042.

Therefore, *Sadjadpour* only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. *Sadjadpour*, however, fails to disclose or suggest selecting a bit loading sequence with the lowest error rate. Appellants respectfully submit that there is simply no disclosure nor suggestion in *Sadjadpour* of any elements which could be comparable to the steps recited in claim 18, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate. As discussed above, and as discussed in Appellants' previous responses, the present invention is directed to a device which contains circuitry and which can perform a step of selecting a bit loading sequence based on a lowest error rate.

Furthermore, Appellants submit that *Sadjadpour* fails to teach or suggest "determining a power allocation for at least one bit loading sequence based on minimizing an error rate," as recited in claim 18. As noted above, *Sadjadpour* does not teach or suggest power allocation for bit loading frequencies based on minimizing the error rate. *Sadjadpour* discloses only power allocation based only on reducing the cross talk. There is no teaching or suggestion in *Sadjadpour* of power allocation for bit loading frequencies based on minimizing the error rate, and as such, Appellants submit that it is incorrect for the final Office Action to suggest or conclude, without specific citation to the prior art, that

Sadjadpour teaches power allocation for bit loading frequencies based on minimizing the error rate when only cross talk is discussed in *Sadjadpour*.

For at least the reasons discussed above, Appellants submit that *Sadjadpour* fails to disclose or suggest all of the elements of claim 18. Accordingly, the Board's consideration and reversal of the rejection thereof is respectfully requested.

3) Claim 23

Claim 23 recites a communication system for transferring data between a transmitter and a receiver over a plurality of channels. The communication system includes a providing means for providing a modulation circuitry having a plurality of modulation alphabets and for providing a set of a bit loading sequences. The system further includes a determining means for determining a power allocation for at least one bit loading sequence based on minimizing an error rate, and selecting means for selecting a bit loading sequence with a lowest error rate.

Appellants respectfully submit that claim 23 recites subject matter which is neither disclosed nor suggested by *Sadjadpour*.

As discussed above, *Sadjadpour* discloses a discrete multi-tone modem that operates to minimize cross talk over a twisted pair cable. The spectrum of the twisted pair cable can be split into multiple sub-bands or QAM channels, where each channel is able to handle K*i* bits of data, where *i* is the member of the channel (*Sadjadpour*, paragraph [0027]). The bit addition algorithm of *Sadjadpour* describes how an array of different bit allocation settings are ordered in ascending order so that bit allocation can be determined based on the least possible power for the maximum data rate possible or a desired data rate (*Sadjadpour*, paragraphs [0037]-[0038]). Bits are then added and the

process continued until the addition of any further bit in any of the frequency bins violates at least one predetermined constraint, such as power budget, power mask, or maximum number of bits per frame, for example. Further, in another described embodiment of *Sadjadpour*, the method of allocating bits is modified by modifying the incremental power term by a weighting dependent on the frequency of the tone (sub-frequency).

As mentioned above, a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Additionally, the "identical invention must be shown in as complete detail as is contained in the...claim" *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Appellants respectfully assert that the final Office Action has failed to meet these requirements.

In other words, Appellants submit that the final Office Action has failed to establish a prima facie case for anticipation as *Sadjadpour* fails to disclose each and every element of claim 23. For example, *Sadjadpour* does not teach or suggest "determining means for determining a power allocation for at least one bit loading sequence based on minimizing an error rate" and "selecting means for selecting a bit loading sequence with a lowest error rate," as recited in claim 23.

The Office Action took the position that *Sadjadpour* disclosed, at paragraphs 0043-0046, the above-recited limitations of claim 23. However, Appellants respectfully assert that no such disclosure exists in *Sadjadpour*. These paragraphs of *Sadjadpour*, which describe Figure 6, show the various inputs which are required in order to operate the bit allocation algorithm. Thus, blocks 61-68 represent the various objective functions

with the shaded blocks of Figure 6 being those used to reduce the cross talk. Function 64 represents the joint minimization of an arbitrary function of the total power and maximization of the total data rate such as would be achieved using the algorithm described in paragraphs 0036-0038. Similarly, function block 61 shows the functions which apply joint minimization of the cross talk and maximization of the total data rate, as is shown in the method described in paragraphs 0039-0042.

Therefore, *Sadjadpour* only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. *Sadjadpour* fails to disclose or suggest selecting a bit loading sequence with the lowest error rate. Appellants respectfully submit that there is simply no disclosure or suggestion in *Sadjadpour* of any elements which could be comparable to the means recited in claim 23, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate. As discussed above, and as discussed in Appellants' previous responses, the present invention is directed to a device which contains circuitry and which can perform a step of selecting a bit loading sequence based on a lowest error rate.

Furthermore, Appellants submit that *Sadjadpour* fails to teach or suggest "determining means for determining a power allocation for at least one bit loading sequence based on minimizing an error rate," as recited in claim 23. As noted above, *Sadjadpour* does not teach or suggest power allocation for bit loading frequencies based on minimizing the error rate. *Sadjadpour* discloses only power allocation based on reducing the cross talk. *Sadjadpour* does not disclose or suggest power allocation for bit loading frequencies based on minimizing the error rate. As such, Appellants submit that

the final Office Action was in error for concluding, without specific citation to the prior art, that *Sadjadpour* teaches power allocation for bit loading frequencies based on minimizing the error rate when only cross talk is discussed in *Sadjadpour*.

For at least the reasons discussed above, Appellants submit that *Sadjadpour* fails to disclose or suggest all of the elements of claim 23. Accordingly, the Board's consideration and reversal of the rejection thereof is respectfully requested.

B. Claims 2-13, 19, 20, and 22 are not obvious in view of *Sadjadpour* and AAPA

Claims 2-13, 19, 20, and 22 stand rejected under 35 U.S.C. §103(a) as being obvious in view of *Sadjadpour* in view of Applicants' admitted prior art (Fig. 1-2 and [0005]-[0023], hereafter, AAPA). The Office Action took the position that *Sadjadpour* teaches each and every element recited in claims 2-13, 19, 20, and 22, except for the MIMO system. However, the Office Action cites to AAPA as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the cited prior art to generate Appellants' claimed invention.

Appellants respectfully submit that claims 2-13, 19, 20, and 22 recite subject matter which is neither disclosed nor suggested by the combination of *Sadjadpour* and AAPA, and as such, the Board's reversal of the rejection is respectfully requested.

1) Claim 2

Claim 2 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 2 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim

allowed.

2) Claim 3

Claim 3 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 3 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

3) Claim 4

Claim 4 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 4 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

4) Claim 5

Claim 5 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 5 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

5) Claim 6

Claim 6 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 6 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations.

Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

6) Claim 7

Claim 7 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 7 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

7) Claim 8

Claim 8 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 8 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

8) Claim 9

Claim 9 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 9 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

9) Claim 10

Claim 10 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 10 is patentable at least for the

reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

10) Claim 11

Claim 11 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 11 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

11) Claim 12

Claim 12 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 12 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

12) Claim 13

Claim 13 is dependent upon claim 1, and recites further limitations. The AAPA does not cure the deficiencies of *Sadjadpour*. Thus, claim 13 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

13) Claim 19

Claim 19 recites a communication system for transferring data between a

transmitter and receiver over a communication channel (Specification, paragraphs 0026, Figures 1-3). The system includes a first circuitry means for decomposing a communication channel into a plurality of logical channels (Specification, paragraphs 0026, 0032, Figures 1-3), and a modulation circuitry having a plurality of modulation alphabets, at least two modulation alphabets are capable of representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels (Specification, paragraphs 0026, 0036-0037, Figures 1-3). The circuitry also includes a second circuitry means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences (Specification, paragraphs 0026, 0043, 0050-0054, Figures 1-3), and a third circuitry for choosing a bit loading sequence having a minimum bit error rate (Specification, paragraphs 0026, 0055-0056, Figures 1-3).

In rejecting claims under 35 USC §103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. In re Fine, 837 F.2d 1071,1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In doing so, the PTO is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966), and to provide a reason why one of ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reasons must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. F-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988), cert. denied, 488 U.S.825 (1988);

Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F2d. 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the PTO are an essential part of complying with the burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Further, to establish prima facie obviousness of a claimed invention, all the claimed limitations must be suggested or taught by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1970). All words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

If the PTO fails to meet this burden, the Applicant is entitled to a patent. In re Glaug, 62 USPQ2d 1151 (Fed. Cir. 2002). In the present case, discussed in detail below, Appellants respectfully submit the PTO has failed to meet this burden.

Appellants' submit that claim 19 recites subject matter that is not taught, shown, or suggested by the cited combination of prior art references. *Sadjadpour* is discussed above and AAPA can be found at paragraphs [0005]-[0023] of Appellants' specification.

Sadjadpour does not teach or suggest "a third circuitry for choosing a bit loading sequence having a minimum error rate," as recited in claim 19. As discussed above, *Sadjadpour* only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. *Sadjadpour*, however, fails to disclose or suggest third circuitry for choosing a bit loading sequence having a minimum bit error rate. Appellants respectfully submit

that there is simply no disclosure or suggestion in *Sadjadpour* of any elements which could be comparable to the third circuitry as recited in claim 19, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate.

Further, Appellants submit that the cited portions of Appellants' specification (paragraphs [0005]-[0023]) also do not teach, show, or suggest "a third circuitry for choosing a bit loading sequence having a minimum error rate," as recited in claim 19. As such, Appellants submit that AAPA does not further the teaching of *Sadjadpour* to the level necessary to properly support an obviousness rejection of claim 19.

The combination of *Sadjadpour* and AAPA fails to disclose or suggest all of the elements of claim 19. Therefore, reconsideration and withdrawal of the rejection of these claims is respectfully requested.

14) Claim 20

Claim 20, upon which claim 21 is dependent, recites a method for transferring data between a transmitter and receiver over a communication channel. The method includes decomposing a communication channel into a plurality of logical channels, and selecting from a plurality of modulation alphabets, wherein at least two modulation alphabets for modulating data are capable of representing the data using a different number of bits. The method further includes identifying a set of bit loading sequences for a fixed data rate which specify a number of bits to be loaded onto corresponding logical channels of the plurality of channels, allocating a power weighting to the corresponding logical channel

for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences, and choosing a bit loading sequence having a minimum bit error rate.

To establish prima facie obviousness of a claimed invention, all the claimed limitations must be suggested or taught by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1970). All words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Appellants' submit that claim 20 recites subject matter that is not taught, shown, or suggested by the cited combination of prior art references. *Sadjadpour* is discussed above and AAPA can be found at paragraphs [0005]-[0023] of Appellants' specification.

Sadjadpour does not teach or disclose allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based on minimizing an error rate, as recited in claim 20. As discussed above, *Sadjadpour* only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. *Sadjadpour*, however, fails to disclose or suggest allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences and choosing a bit loading sequence having a minimum bit error rate. Appellants respectfully submit that there is simply no disclosure or suggestion in *Sadjadpour* of any elements which could be comparable to the allocating and choosing steps recited in claim 20, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate.

Further, Appellants submit that the cited portions of Appellants' specification (paragraphs [0005]-[0023]) also do not teach, show, or suggest the limitations recited in claim 20. More particularly, Appellants submit that AAPA does not teach allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based on minimizing an error rate. As such, Appellants submit that AAPA does not further the teaching of *Sadjadpour* to the level necessary to properly support an obviousness rejection of claim 20.

Appelants, therefore, respectfully assert that the combination of *Sadjadpour* and AAPA does not disclose or suggest all of the elements of claim 20. Thus, reconsideration and withdrawal of the rejection of claim 20 is respectfully requested.

15) Claim 22

Claim 22 recites a communication system for transferring data between a transmitter and receiver over a communication channel. The system includes a decomposing means for decomposing a communication channel into a plurality of logical channels, and a representing means for representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels. The system further includes an allocating means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences, and a choosing means for choosing a bit loading sequence having a minimum bit error rate.

To establish prima facie obviousness of a claimed invention, all the claimed limitations must be suggested or taught by the prior art. In re Royka, 490 F.2d 981, 180

USPQ 580 (CCPA 1970). All words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Appellants submit that claim 22 recites subject matter that is not taught, shown, or suggested by the cited combination of prior art references. *Sadjadpour* is discussed above and AAPA can be found at paragraphs [0005]-[0023] of Appellants' specification.

Sadjadpour does not teach or disclose allocating means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences and choosing means for choosing a bit loading sequence having a minimum bit error rate, as recited in claim 22. As discussed above, *Sadjadpour* only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. *Sadjadpour*, however, fails to disclose or suggest allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences and choosing a bit loading sequence having a minimum bit error rate. Appellants respectfully submit that there is simply no disclosure or suggestion in *Sadjadpour* of any elements which could be comparable to the allocating means and choosing means recited in claim 22, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate.

Further, Appellants submit that the cited portions of Appellants' specification (paragraphs [0005]-[0023]) also do not teach, show, or suggest the limitations recited in claim 20. More particularly, Appellants submit that AAPA does not teach allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading

sequence and choosing at least one bit loading sequence based on minimizing an error rate. As such, Appellants submit that AAPA does not further the teaching of *Sadjadpour* to the level necessary to properly support an obviousness rejection of claim 22.

Appellants, therefore, respectfully assert that the combination of *Sadjadpour* and AAPA does not disclose or suggest all of the elements of claim 22. Thus, reconsideration and withdrawal of the rejection of claim 22 is respectfully requested.

With regard to each of the obviousness rejections discussed above, Appellants submit that in addition to the above noted remarks, Appellants further note that the method shown in the description of *Sadjadpour* is specifically related to the problem of cross talk in twisted pair modems, and as such, the method of *Sadjadpour* describes a weighting algorithm to reduce cross talk based on twisted pair cross talk algorithms. Appellants note that even if a person of skill in the art were to examine the teaching of *Sadjadpour*, they would not have considered *Sadjadpour* to be a suitable starting point for generating Appellants' claimed invention, as fields of wired and wireless communication are significantly different in most aspects. Appellants submit that one of skill in the art working in a twisted pair environment would not look to a wireless solution to solve a twisted pair problem. Thus, Appellants submit that in the absence of any teaching, suggestion, or motivation to do so found in the references themselves, a person skilled in the art would not have considered modifying a twisted pair modem communication technique for application in a wireless communication system, and combination of such teachings is inappropriate. Thus, Appellants submit that the references cited in support of the §103 rejection are not properly combined, and reconsideration and withdrawal of the obviousness rejections is respectfully requested.

C. Claims 14-17 and 21 are not obvious in view of *Sadjadpour*, AAPA, and Kim

Claims 14-17 and 21 were rejected under 35 U.S.C. §103(a) as being obvious in view of *Sadjadpour* in view of AAPA, further in view of *Kim* (U.S. Publication No. 2003/0128769). The Office Action took the position that *Sadjadpour* teaches each and every element recited in claims 14-17 and 21, except for codings and modulations that utilize system bits. However, the Office Action cites to *Kim* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Appellants' claimed invention.

Sadjadpour and AAPA are discussed above. *Kim* discloses a method for providing first and second interleaved bit streams to a modulator in order to transmit the first and second interleaved bit streams through at least two antennas in a mobile communication system. An encoder encodes a transmission data stream into a first bit stream with first priority and a second bit stream with second priority being lower than the first priority. An interleaver interleaves the first and second bit streams into the first and second interleaved bit streams. The modulator modulates the first and second interleaved bit streams.

Appellants respectfully submit that the combination of *Sadjadpour,* AAPA, and *Kim* fails to disclose or suggest all of the elements of claims 14-17 and 21. In rejecting claims under 35 USC §103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. In re Fine, 837 F.2d 1071,1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In doing so, the PTO is expected to make the

factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966), and to provide a reason why one of ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reasons must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. F-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988), cert. denied, 488 U.S.825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F2d. 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the PTO are an essential part of complying with the burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Further, to establish prima facie obviousness of a claimed invention, all the claimed limitations must be suggested or taught by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1970). All words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

If the PTO fails to meet this burden, the Applicant is entitled to a patent. In re Glaug, 62 USPQ2d 1151 (Fed. Cir. 2002). In the present case, discussed in detail below, Appellants respectfully submit the PTO has failed to meet this burden.

1) Claim 14

Claim 14 is dependent upon claim 1, and recites further limitations. As discussed

above, AAPA and *Sadjadpour* do not disclose or suggest all of the limitations of claim 1. Additionally, *Kim* does not teach, show, or suggest circuitry configured to select a bit loading sequence with a lowest error rate, as recited in claim 14. Thus, claim 14 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

2) Claim 15

Claim 15 is dependent upon claim 1, and recites further limitations. As discussed above, AAPA and *Sadjadpour* do not disclose or suggest all of the limitations of claim 1. Additionally, *Kim* does not teach, show, or suggest circuitry configured to select a bit loading sequence with a lowest error rate, as recited in claim 15. Thus, claim 15 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

3) Claim 16

Claim 16 is dependent upon claim 1, and recites further limitations. As discussed above, AAPA and *Sadjadpour* do not disclose or suggest all of the limitations of claim 1. Additionally, *Kim* does not teach, show, or suggest circuitry configured to select a bit loading sequence with a lowest error rate, as recited in claim 16. Thus, claim 16 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

4) Claim 17

Claim 17 is dependent upon claim 1, and recites further limitations. As discussed above, AAPA and *Sadjadpour* do not disclose or suggest all of the limitations of claim 1. Additionally, *Kim* does not teach, show, or suggest circuitry configured to select a bit loading sequence with a lowest error rate, as recited in claim 17. Thus, claim 17 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

5) Claim 21

Claim 21 is dependent upon claim 20, and recites further limitations. As discussed above, the combination of AAPA and *Sadjadpour* do not disclose or suggest all of the limitations of claim 20. Additionally, *Kim* does not teach or disclose allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based on minimizing an error rate, as recited in claim 20. Thus, claim 21 is patentable at least for the reasons claim 20 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

For all of the above noted reasons, it is strongly contended that certain clear differences exist between the present invention as claimed in claims 1-23 and the prior art relied upon by the Examiner. It is further contended that these differences are more than sufficient that the present invention would not have been obvious to a person having ordinary skill in the art at the time the invention was made.

This final rejection being in error, therefore, it is respectfully requested that this

honorable Board of Patent Appeals and Interferences reverse the Examiner's decision in this case and indicate the allowability of application claims 1-23.

In the event that this paper is not being timely filed, the Appellants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees which may be due with respect to this paper may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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Encls: Appendix 1 - Claims on Appeal
Appendix 2 - Evidence
Appendix 3 - Related Proceedings
Appendix 4 - Drawings

APPENDIX 1

CLAIMS ON APPEAL

1. (Previously Presented) A communication system for transferring data between a transmitter and a receiver over a plurality of channels, the communication system comprising:

modulation circuitry having a plurality of modulation alphabets providing a set of bit loading sequences;

circuitry configured to determine a power allocation for at least one bit loading sequence based on minimizing an error rate; and

circuitry configured to select a bit loading sequence with a lowest error rate.

2. (Original) The communication system according to claim 1, wherein the plurality of channels comprises independent logical channels decomposed from a Multiple-Input, Multiple-Output channel.

3. (Original) The communication system according to claim 1, wherein the plurality of channels comprises independent logical channels decomposed from an orthogonal frequency division multiplexing channel.

4. (Original) The communication system according to claim 1, wherein the plurality of modulation alphabets is capable of representing data using a different number of bits.

5. (Original) The communication system according to claim 4, wherein for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded on at least one channel of the plurality of channels.

6. (Original) The communication system according to claim 5, wherein the fixed data rate is selected based on a channel quality indicator.

7. (Original) The communication system according to claim 6, wherein the channel quality indicator is calculated at the transmitter.

8. (Original) The communication system according to claim 6, wherein the channel quality indicator is calculated at the receiver.

9. (Original) The communication system according to claim 1, wherein the determined power allocation provides a power weighting for at least one channel of the plurality of channels.

10. (Original) The communication system according to claim 9, wherein if an identical modulation alphabet is used for at least two logical channels then a greater power weighting is allocated to weaker logical channels.

11. (Original) The communication system according to claim 1, wherein a power allocation used to transfer the data comprises the power allocation determined for the at least one bit loading sequence.

12. (Original) The communication system according to claim 1, wherein the transmitter comprises a plurality of transmitting antennas.

13. (Original) The communication system according to claim 1, wherein the receiver comprises a plurality of receiving antennas.

14. (Original) The communication system according to claim 1, further comprising coding circuitry for adding parity bits to system bits and for distinguishing between the parity bits and the system bits.

15. (Original) The communication system according to claim 14, wherein the parity bits are transferred on a weak channel.

16. (Original) The communication system according to claim 14, wherein for a bit loading sequence having an identical modulation alphabet on at least two channels of the plurality of channels, the parity bits are transferred on at least one of a weakest channel and the power allocation is reduced.

17. (Original) A system according to claim 14, wherein for a bit loading sequence having different modulation alphabets on the plurality of channels, the parity bits are transferred in a least significant bits of a modulation alphabet used on a strong channel.

18. (Original) A method for transferring data between a transmitter and receiver over a communication channel, the method comprising:

identifying a set of bit loading sequences from a plurality of modulation alphabets;

determining a power allocation for at least one bit loading sequence based on minimizing an error rate; and

selecting a bit loading sequence with a lowest error rate and applying the power allocation to at least one communication channel.

19. (Original) A communication system for transferring data between a transmitter and receiver over a communication channel, the system comprising:

a first circuitry means for decomposing a communication channel into a plurality of logical channels;

modulation circuitry having a plurality of modulation alphabets, at least two modulation alphabets are capable of representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels;

a second circuitry means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences; and

a third circuitry for choosing a bit loading sequence having a minimum bit error rate.

20. (Original) A method for transferring data between a transmitter and receiver over a communication channel, the method comprising:

decomposing a communication channel into a plurality of logical channels;

selecting from a plurality of modulation alphabets, wherein at least two modulation alphabets for modulating data are capable of representing the data using a different number of bits;

identifying a set of bit loading sequences for a fixed data rate which specify a number of bits to be loaded onto corresponding logical channels of the plurality of channels;

allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences; and

choosing a bit loading sequence having a minimum bit error rate.

21. (Original) A method according to claim 20, wherein the data to be transferred comprises systematic bits and parity bits, and wherein the parity bits are loaded onto weaker logical channels.

22. (Original) A communication system for transferring data between a transmitter and receiver over a communication channel, the system comprising:

decomposing means for decomposing a communication channel into a plurality of logical channels;

representing means for representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels;

allocating means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences; and

choosing means for choosing a bit loading sequence having a minimum bit error rate.

23. (Original) A communication system for transferring data between a transmitter and a receiver over a plurality of channels, the communication system comprising:

providing means for providing a modulation circuitry having a plurality of modulation alphabets and for providing a set of bit loading sequences;

determining means for determining a power allocation for at least one bit loading sequence based on minimizing an error rate; and

selecting means for selecting a bit loading sequence with a lowest error rate.

APPENDIX 2

EVIDENCE APPENDIX

No evidence under section 37 C.F.R. 1.130, 1.131, or 1.132 has been entered or will be relied upon by Appellants in this appeal.

APPENDIX 3

RELATED PROCEEDINGS APPENDIX

No decisions of the Board or of any court have been identified under 37 C.F.R. §41.37(c)(1)(ii).

APPENDIX 4

DRAWINGS OF APPLICATION SERIAL NO. 10/632,089

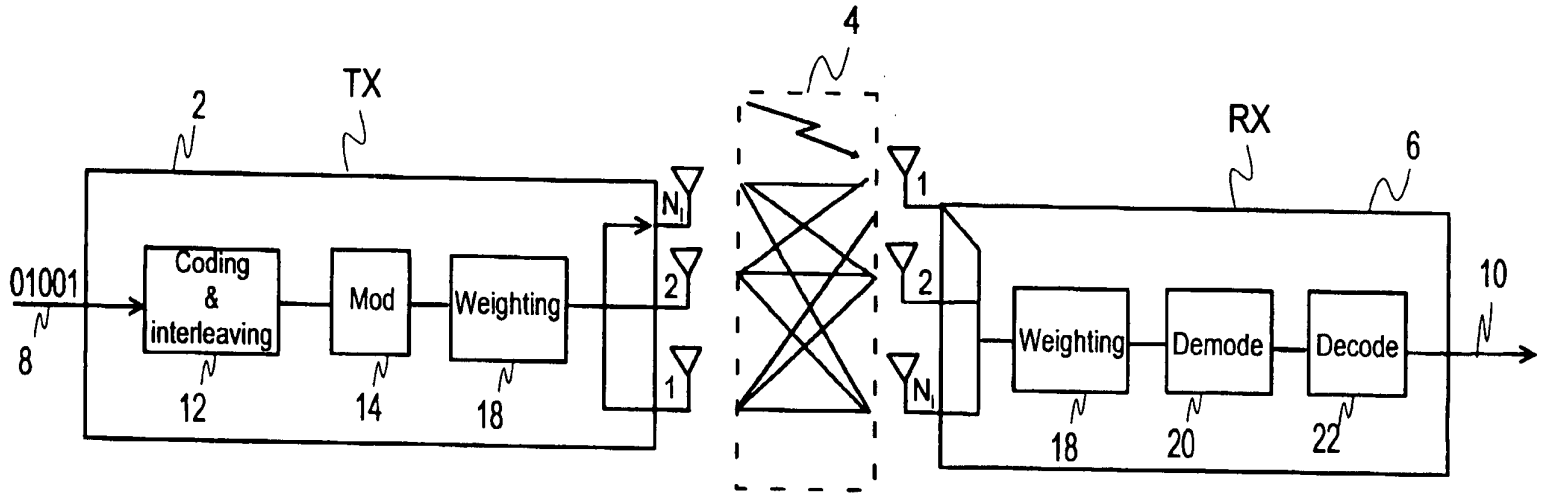

Fig. 1

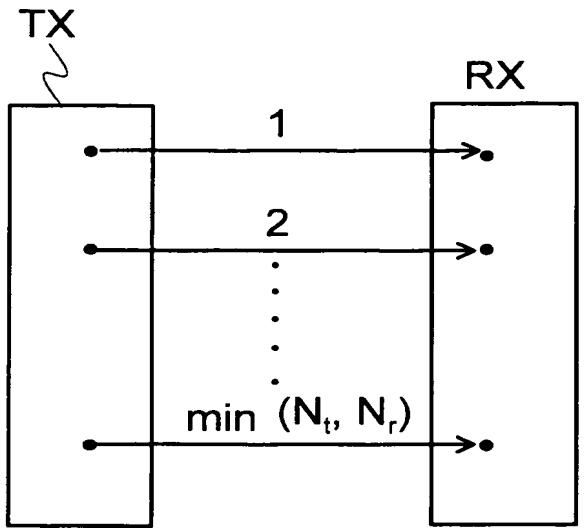

Fig. 2

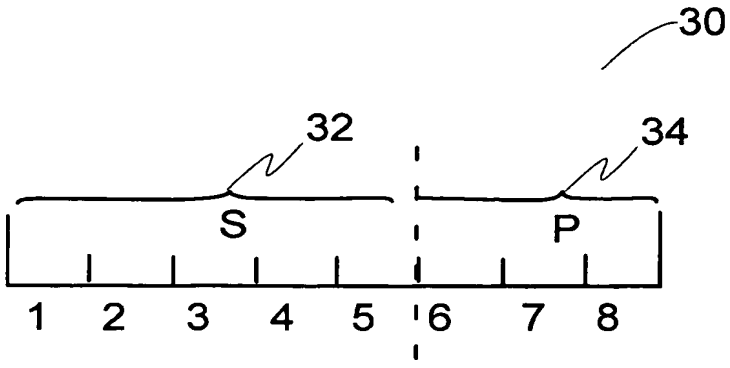

Fig. 3